Claims

[c1] 1. A method for fabricating a flash memory, comprising the steps of:
forming a stacked gate structure and a source/drain on a substrate;
forming an inter-layer dielectrics on the substrate; and
forming a plurality of inter-metal dielectric layers on the substrate, wherein at least one layer among the inter-layer dielectrics and the inter-metal dielectric layers has a silicon carbide layer formed thereon.

[c2] 2. The method of claim 1, wherein a thickness of the silicon carbide layer ranges from about 100 Å to about 1000 Å .

[c3] 3. The method of claim 1, wherein a thickness of the silicon carbide layer ranges from about 300 Å to about 500 Å .

[c4] 4. The method of claim 1, wherein forming the stacked gate structure comprises:
forming a composite dielectric layer on the substrate;
forming a gate conductive layer on the composite dielectric layer; and
patterning the gate conductive layer and the composite dielectric layer.

[c5] 5. The method of claim 4, wherein the composite dielectric layer comprises a tunnel oxide layer, a silicon nitride layer, and a silicon oxide layer.

[c6] 6. The method of claim 4, wherein the gate conductive layer comprises a doped polysilicon layer and a metal silicide layer.

[c7] 7. The method of claim 4, wherein the method for forming the gate conductive layer comprises chemical vapor deposition (CVD).

[c8] 8. A method for fabricating a flash memory, comprising the steps of:
forming a stacked gate structure and a source/drain on a substrate;
forming an inter-layer dielectrics on the substrate; and
forming a silicon carbide layer on the inter-layer dielectrics.

[c9] 9. The method of claim 8, wherein a thickness of the silicon carbide layer ranges from about 100 Å to about 1000 Å .

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[c10] 10. The method of claim 8, wherein a thickness of the silicon carbide layer ranges from about 300 Å to about 500 Å .

[c11] 11. The method of claim 8, wherein forming the stacked gate structure comprises:
forming a silicon oxide/silicon nitride/silicon oxide (ONO) composite layer on the substrate;
forming a gate conductive layer on the ONO composite layer; and
patterning the gate conductive layer and the ONO composite layer.

[c12] 12. The method of claim 11, wherein the gate conductive layer comprises a doped polysilicon layer and a metal silicide layer.

[c13] 13. A method for fabricating a flash memory, comprising the steps of:
forming a stacked gate structure and a source/drain on a substrate;
forming an inter-layer dielectrics on the substrate;
forming a contact in the inter-layer dielectrics;
forming a metal interconnection on the inter-layer dielectrics;
forming an inter-metal dielectrics on the substrate; and
forming a first silicon carbide layer on the inter-metal dielectrics.

[c14] 14. The method of claim 13, further comprising forming a second silicon carbide layer on the inter-layer dielectrics before the contact is formed in the inter-layer dielectrics.

[c15] 15. The method of claim 14, wherein a thickness of the first and the second silicon carbide layers ranges from about 100 Å to about 1000 Å .

[c16] 16. The method of claim 14, wherein a thickness of the first and the second silicon carbide layer ranges from about 300 Å to about 500 Å .

[c17] 17. The method of claim 13, wherein forming the stacked gate structure comprises:
forming a silicon oxide/silicon nitride/silicon oxide (ONO) composite layer on the substrate;
forming a gate conductive layer on the ONO composite layer; and

patterning the gate conductive layer and the ONO composite layer.

[c18] 18. The method of claim 17, wherein the gate conductive layer comprises a doped polysilicon layer and a metal silicide layer.

[c19] 19. The method of claim 18, wherein the metal silicide layer comprises a tungsten silicide layer.

[c20] 20. The method of claim 17, wherein the method for forming the gate conductive layer comprises chemical vapor deposition (CVD).

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